IN THE SPECIFICATION

Please replace the paragraph beginning at line 15, page 6 with the following rewritten paragraph:

Turning now to FIG. 2, a schematic block diagram of a computer system 200 capable of executing a lithography simulation tool 210, a layout test pattern generator [[215]] 225, and other design processes using electronic design automation (EDA) tools [[225]] 215 in accordance with the present invention is illustrated. As indicated, the simulation tool 210 can be used to generate a simulation image and identify portions of a layout including structures exhibiting or otherwise demonstrating poor manufacturability. In one embodiment, the simulation tool 210 is embodied as a computer program (e.g., a software application including a compilation of executable code). As described more fully below, the layout test pattern generator [[215]] 225 can be used to generate a plurality of parametrically varying layout test patterns.

Please replace the paragraph beginning at line 26, page 6 and ending at line 6, page 7 with the following rewritten paragraph:

To execute the simulation tool 210 and /or the layout test pattern generator [[215]] 225, the computer system 200 can include one or more processors 220 used to execute instructions that carry out a specified logic routine. In addition, the computer system 200 can include a memory 230 for storing data, software, logic routine instructions, computer programs, files, operating system instructions, and the like. The memory 230 can comprise several devices and includes, for example, volatile and non-volatile memory components. As used herein, the memory 230 can include, for example, random access memory (RAM), read-only memory (ROM), hard disks, floppy disks, compact disks (e.g., CD-ROM, DVD-ROM, CD-RW, etc.), tapes, and/or other memory components, plus associated drives and players for these memory types. The processor 220 and the memory 230 are coupled using a local interface 240. The local interface 240 can be, for example, a data bus, accompanying control bus, a network, or other subsystem.

Please replace the Abstract with the following rewritten paragraph:

A method of producing design rules [[can]] including generating a plurality of parametrically varying geometric layouts and simulating how each geometric layout will pattern on a wafer. Edges of structures within the simulated geometric layouts can be classified based on manufacturability and design rules can be created to disallow layouts demonstrating poor manufacturability.